Amendments to the Claims:

This Listing of Claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1-15 (canceled).

16. (new) A method of manufacturing a semiconductor device comprising:

a preparation step including:

preliminarily forming on a sample wafer a test pattern having three-dimensional line and space patterns and an actual circuit pattern having three dimensional portions while varying a process parameter in the semiconductor manufacturing process used to make the sample wafer;

using an optical scatterometry apparatus, measuring a feature of the test pattern and a feature of a critical predetermined portion of the actual circuit pattern; and

calculating a first correspondence relationship between the feature of the test pattern and the feature of the actual circuit pattern, and a second correspondence relationship between the process parameter and the measured features; and

an evaluation step including:

measuring a feature of the test pattern by use of the optical scatterometry apparatus;

determining a process parameter based on the first correspondence relationship;

estimating an amount of the critical portion based on the second correspondence relationship; and

evaluating the semiconductor manufacturing process for the actual circuit pattern based on the estimated amount.

17. (new) A method as in claim 16 wherein the optical scatterometry apparatus comprises an atomic force microscope or a scanning electron microscope.

18. (new) A method as in claim 16 wherein in the preparation step and the evaluation step the semiconductor manufacturing process comprises a semiconductor exposure and development step, and the process parameter includes at least one of exposure and focus.

19. (new) A method as in claim 16 wherein in the preparation step and the evaluation step, the semiconductor manufacturing process includes a semiconductor etching process, and the process parameter comprises at least one of gas flow rate, pressure variation, and etching time.

20. (new) A method as in claim 16 wherein the evaluation step includes a step of displaying the process parameter on a process window as a range of process parameters with a plurality of circuit patterns, and the process window is determined based upon the second correspondence relationship.

21. (new) A method of manufacturing a semiconductor device comprising:

a preparation step including the steps of preliminarily forming on a sample wafer a three-dimensional test pattern having line and space patterns and an actual circuit pattern, while varying a process parameter of the manufacturing process;

measuring features of the three-dimensional shape of the test pattern by using an optical scatterometry apparatus;

measuring features of the three-dimensional shape of a critical portion of the actual circuit pattern by using the optical scatterometry apparatus while also varying process parameters; and

calculating a first correspondence relationship between the measured features of the test pattern and the varying process parameters, and a second correspondence relationship between the varied process parameters and the measured features of the critical portion of the actual circuit pattern.

22. (new) A system for manufacturing a semiconductor device comprising:

a preparation unit for preliminarily measuring for a plurality of sample wafers, each provided with a test pattern having line and space patterns, and each having an actual circuit pattern formed while varying a process parameter in the semiconductor manufacturing process, features of the three-dimensional test pattern by using an optical scatterometry apparatus and features of a critical portion of the actual circuit pattern by using the optical scatterometry apparatus, and calculating a first correspondence relationship between the measured features of the three-dimensional test pattern and the varied process parameters, and a second correspondence relationship between the varied process parameters and the measured features of the critical portion of the actual circuit pattern; and

an evaluation unit for using the optical scatterometry apparatus to measure the test pattern and determine process parameters based on a first correspondence relationship determined by the preparation unit and estimating an amount of the critical portion based on the second correspondence relationship.

23. (new) A system as in claim 22 further comprising a unit for providing feedback of information on the semiconductor manufacturing process to a manufacturing apparatus.

24. (new) The system as in claim 22 wherein the evaluation unit includes a display unit for displaying the process parameters.

25. (new) A system as in claim 22 wherein the evaluation unit includes a display unit for displaying the process parameters on a process window as a range of process parameters for which actual circuit patterns can be formed, the process window being determined based on the second correspondence relationship.

26. (new) A method as in claim 21 wherein the evaluation step includes displaying the determined process parameter on a process window as a range of process parameters for which critical circuit patterns can be formed, the process window being determined based upon the second correspondence relationship.